Innovation in the Semiconductor Industry- Implications for Education and Diversity

IEEE Frontiers in Education Conference

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About Me:

- General Partner, Spirit Ventures
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- BOD member of Thin Film Electronics ASA (Norway and Sweden), and Numascale AS (Norway)
- 15 years in Intel Capital
  - Intel Achievement Award for strategic impact of investments
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- CEO of Translarity Inc., a maker of Probe Cards
- 6 years in Intel Supplier Development Group
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- PhD Chemical Engineering, UC Berkeley
- Degrees/Certificates in Photography and FinTech
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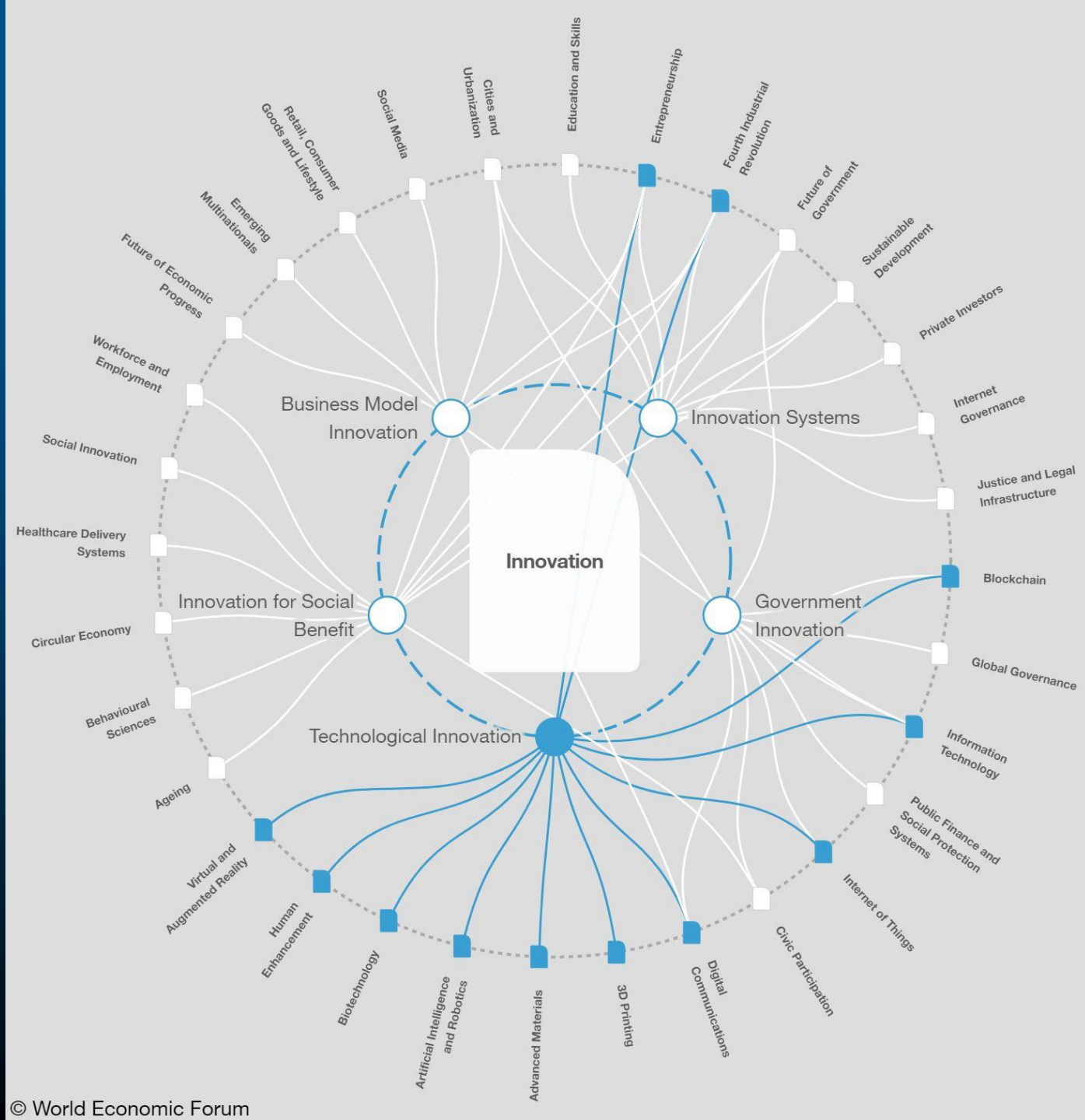
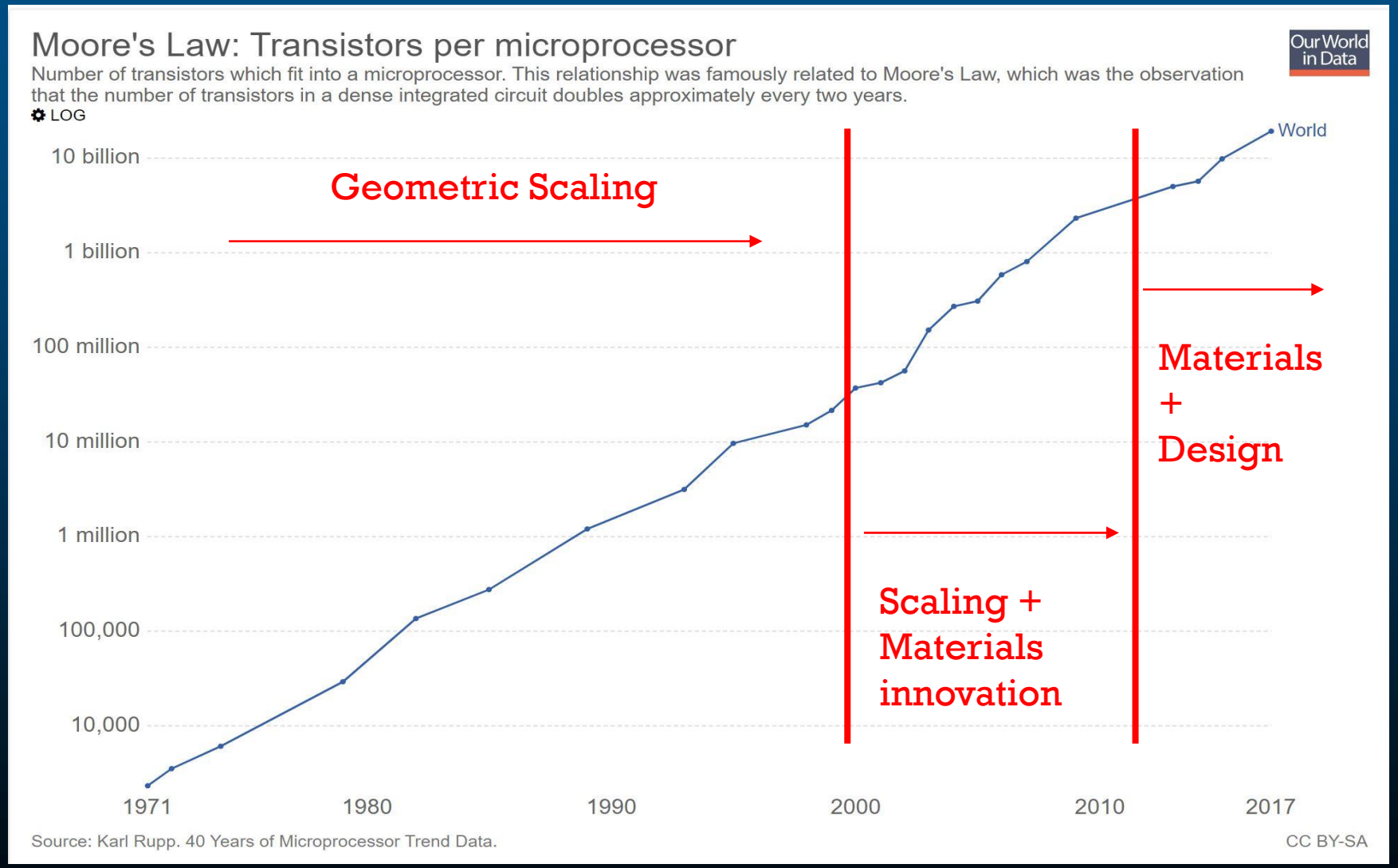
Innovation is Interconnected in the Fourth Industrial Revolution

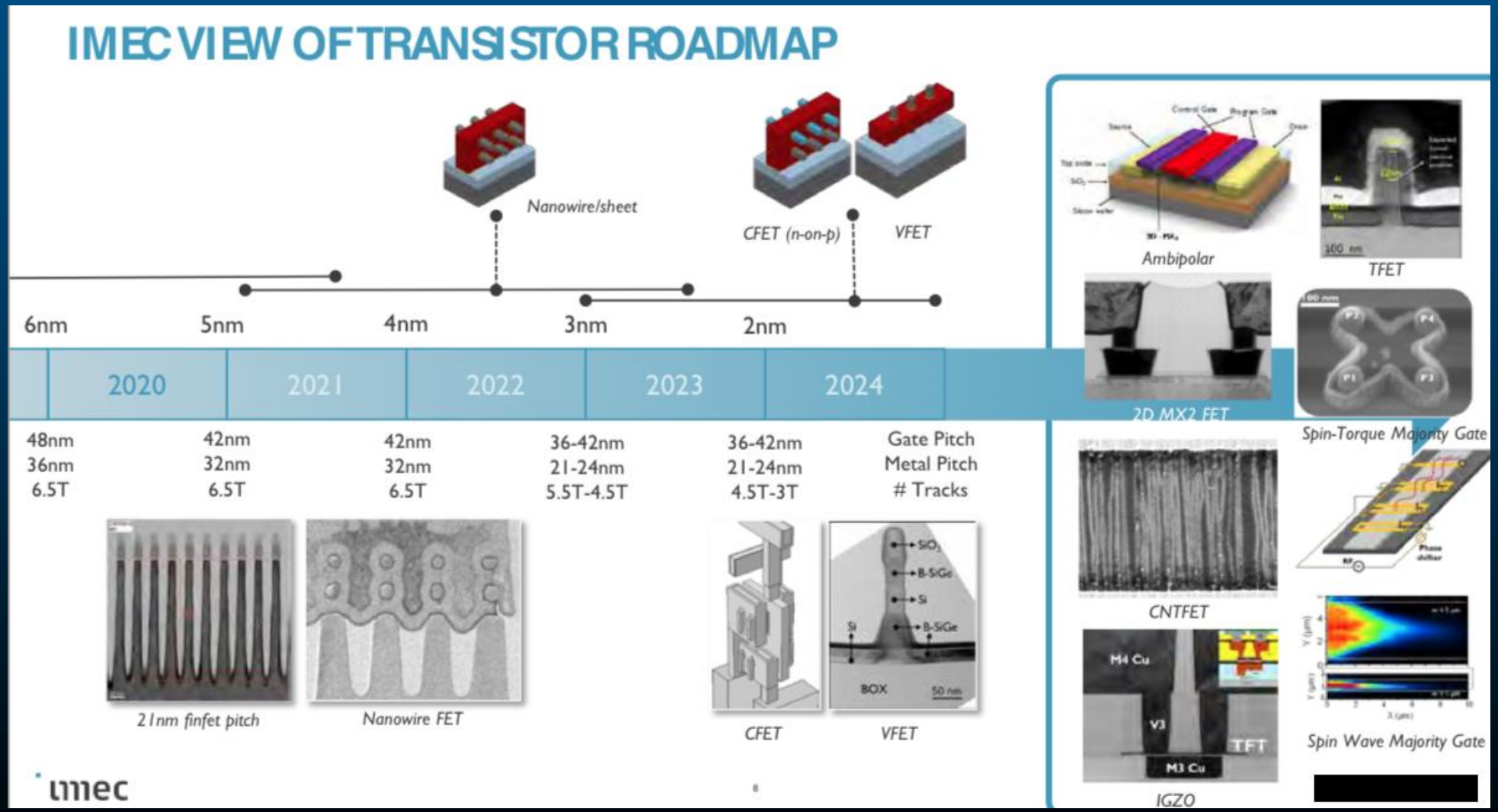


“Moore’s Law”- the Guiding Light of the Semiconductor Industry for Over 50 Years



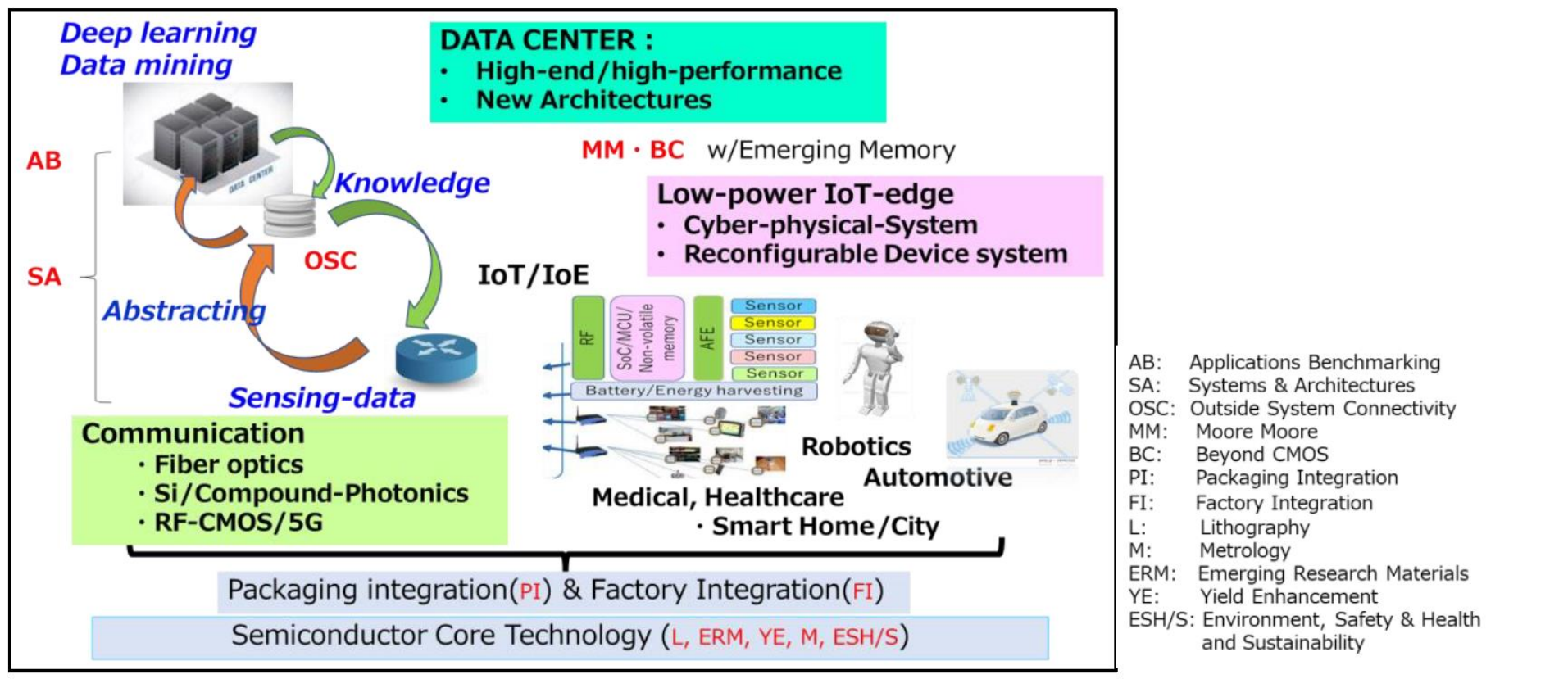
The Future of Moore's Law is Design/Application Innovations

(Source: IMEC and https://semiengineering.com/transistor-options-beyond-3nm)



The Future of Moore's Law is Design/Application Innovations

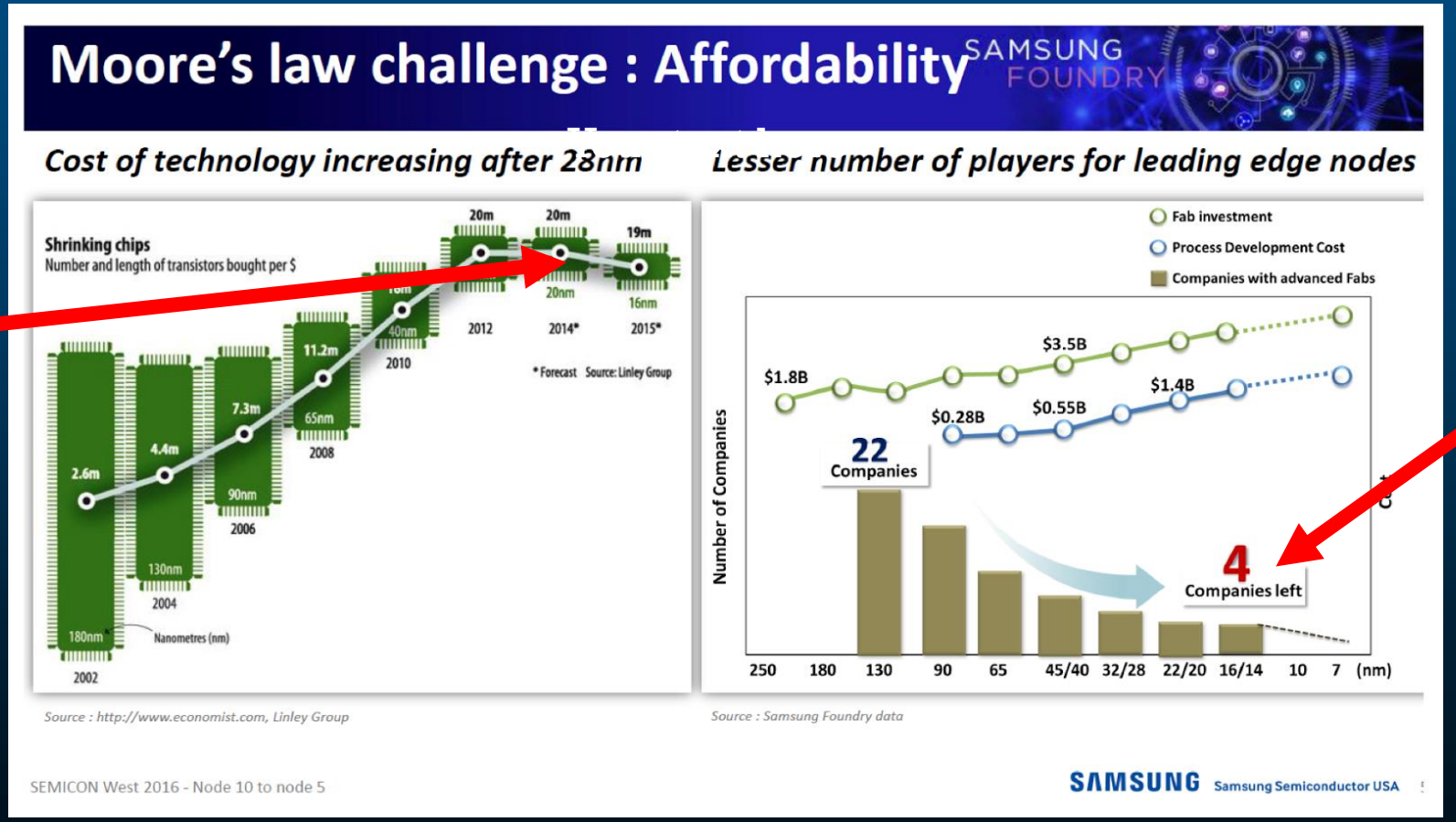
(SOURCE: INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS, 2017)



AB: Applications Benchmarking
SA: Systems & Architectures
OSC: Outside System Connectivity
MM: Moore Moore
BC: Beyond CMOS
PI: Packaging Integration
FI: Factory Integration
L: Lithography
M: Metrology
ERM: Emerging Research Materials
YE: Yield Enhancement
ESH/S: Environment, Safety & Health and Sustainability

But, the Economics are Becoming More Challenging

200 mm process technology increasing to address economic issues



Now 3 companies, with GF announcement of withdrawal from 7 nm development

And…

The Near term Challenges For Moore's Law are Interdisciplinary in Nature

(Source: International Roadmap for Devices and Systems, 2017)

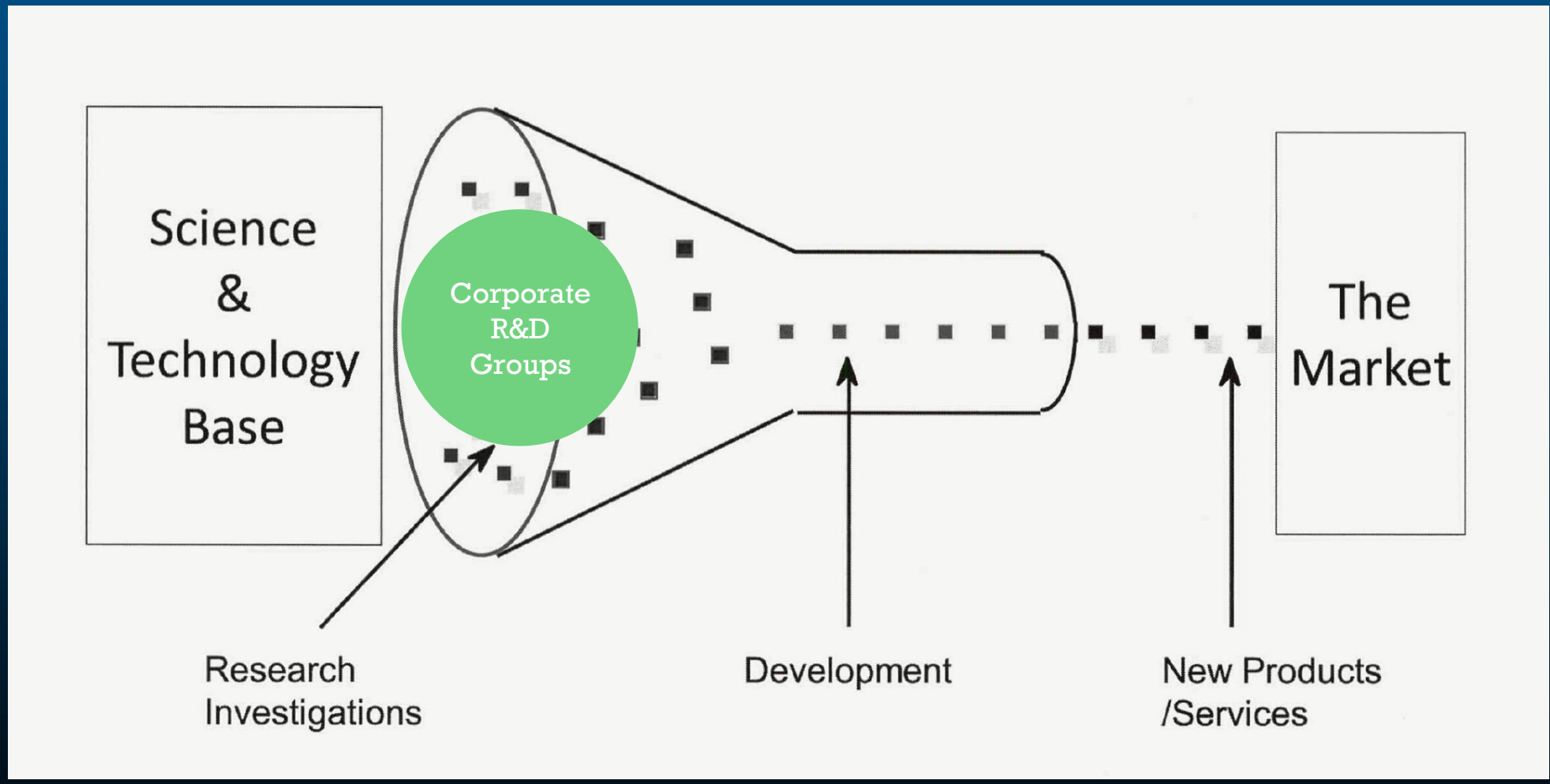
Near-Term Challenges: 2017-2024	Description
Power scaling	Voltage and capacitance scaling slow-down and lack of knobs for power reduction. Introduction of gate-all-around (GAA) devices is a remedy to reduce the supply voltage, but not in a sustained manner that allows continuous scaling. Loading capacitance is now mostly due to the parasitic components of the device that, with continuous scaling of ground rules, cause those components to dominantly form a significant portion of overall capacitance. Therefore, an introduction of low-κ materials, design-technology-co-optimization introducing new contact access schemes as well as local interconnect schemes that allow lower parasitics is needed.
Parasitics scaling	Maintaining control of increased parasitics in vertically stacked devices. Vertical devices require high-aspect ratio contacts to access the bottom contact. This will increase both the contact resistance as well as the fringe capacitance between the gate and drain/source. Interface resistance will also require new silicidation schemes that conformally wrap the source/drain.
Cost reduction	Cost-effective area scaling through EUV and design-technology-co-optimization (DTCO). Throughput and yield challenges of EUV necessitate a careful selection of ground rules that optimizes the die cost as most of the cost is determined by the middle-of-line (MOL) and BEOL stack. Therefore, new design constructs that tighten the secondary design rules such as tip-to-tip and the P-N separation rule are necessary to allow a further shrink of the standard cell and bitcell area on top of ground rule scaling for low-cost die. Process integration of those design constructs might require new materials to allow better etch selectivity and self-deposition.
Integration enablement for SRAM-cache applications	Bitcell scaling is slowing down because of the slow-down of device vertical (e.g. fin pitch) and horizontal pitch (contacted poly pitch). New device schemes such as P-over-N stacked device or vertical devices bring an opportunity to significantly reduce the SRAM area. This is due to the optimized layouts that eliminate the critical design rules impacting the area. Option of embedded NVM in high-performance logic. Being able to integrate most of emerging memories (e.g., MRAM) at the interconnect stack also bring an opportunity for high-density memories. However, the stack as well as the materials should be compatible with the BEOL stack.
Interconnect scalability	Maintaining control of interconnect resistance and EM and TDDB limits. Interconnect resistance has now entered an exponential increase regime because of non-ideal scaling of the barrier for Cu and increased scattering at the surface and grain-boundary interfaces. Therefore, there is need for new barrier materials and Cu alternative solutions. In addition to resistance scalability, time-dependent-dielectric-breakdown (TDDB) is putting a limit on the minimum space between the adjacent lines for a given low-κ dielectric.

Implications for Corporate Innovation

Yesterday's Innovation Ecosystem

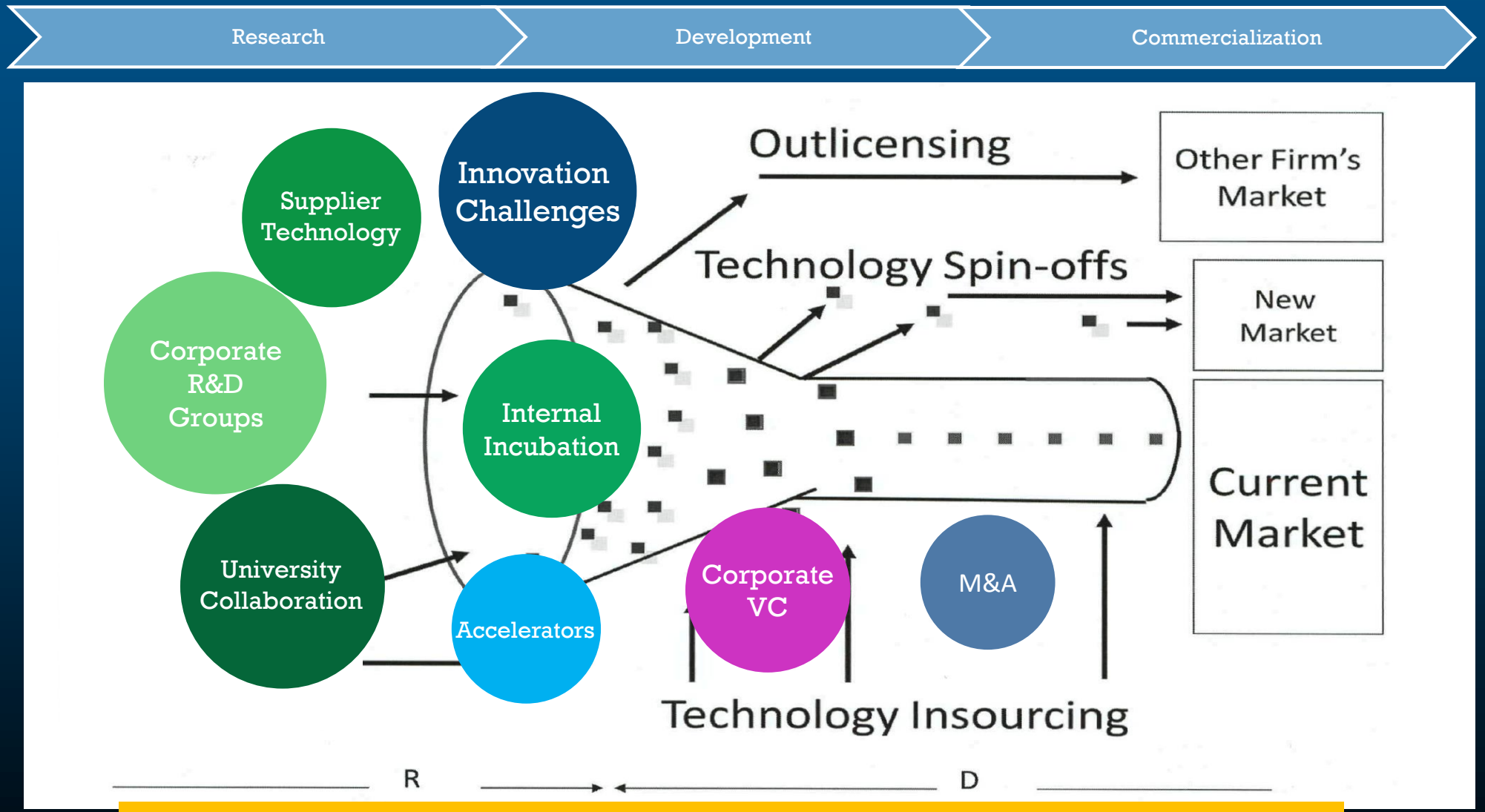
(Source: Chesbrough, 2012)

Research | Development | Commercialization



Today's Innovation Ecosystem

(Source: Chesbrough, 2012)



Problems are Complex, and Industry is Taking a Multipronged Approach

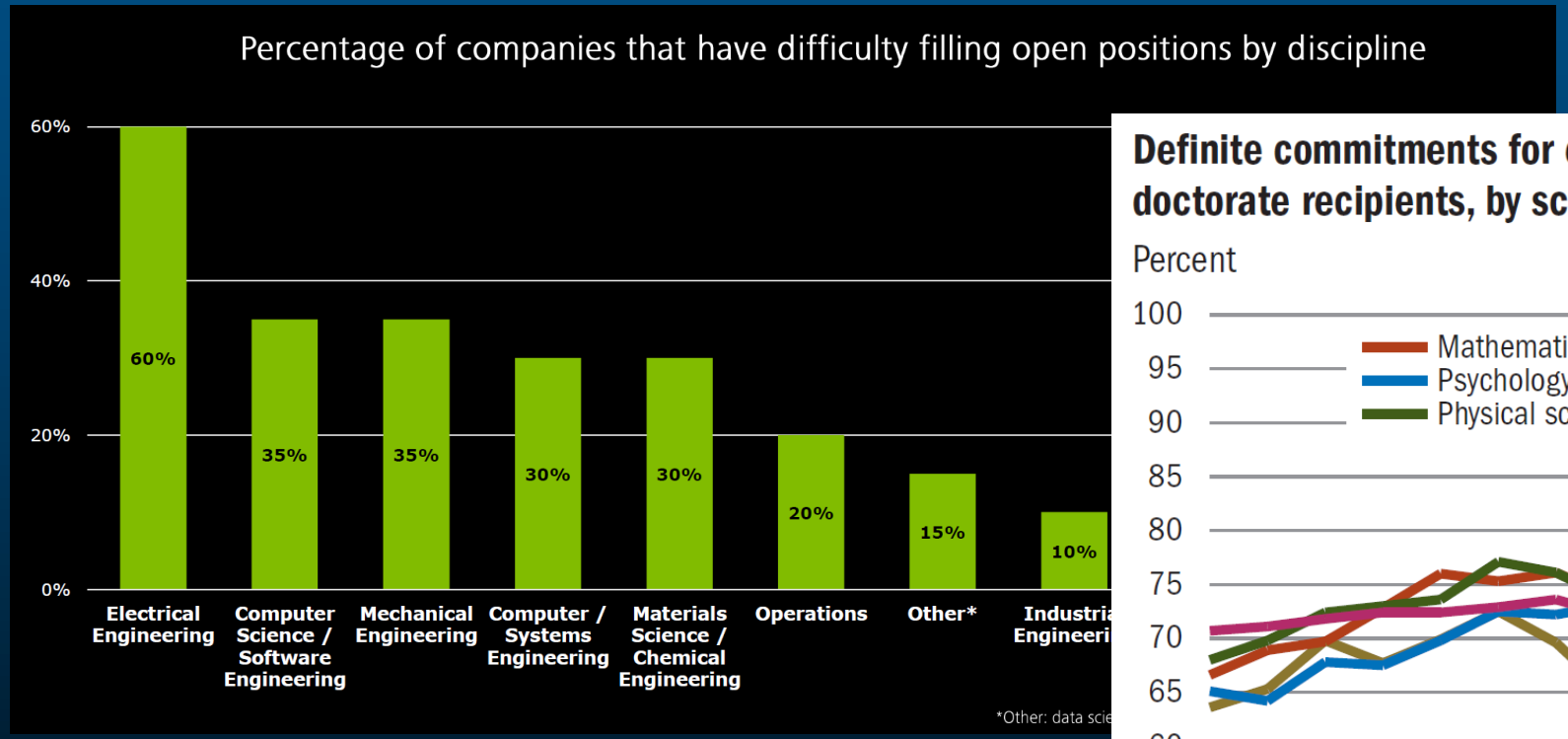
Implications for Education

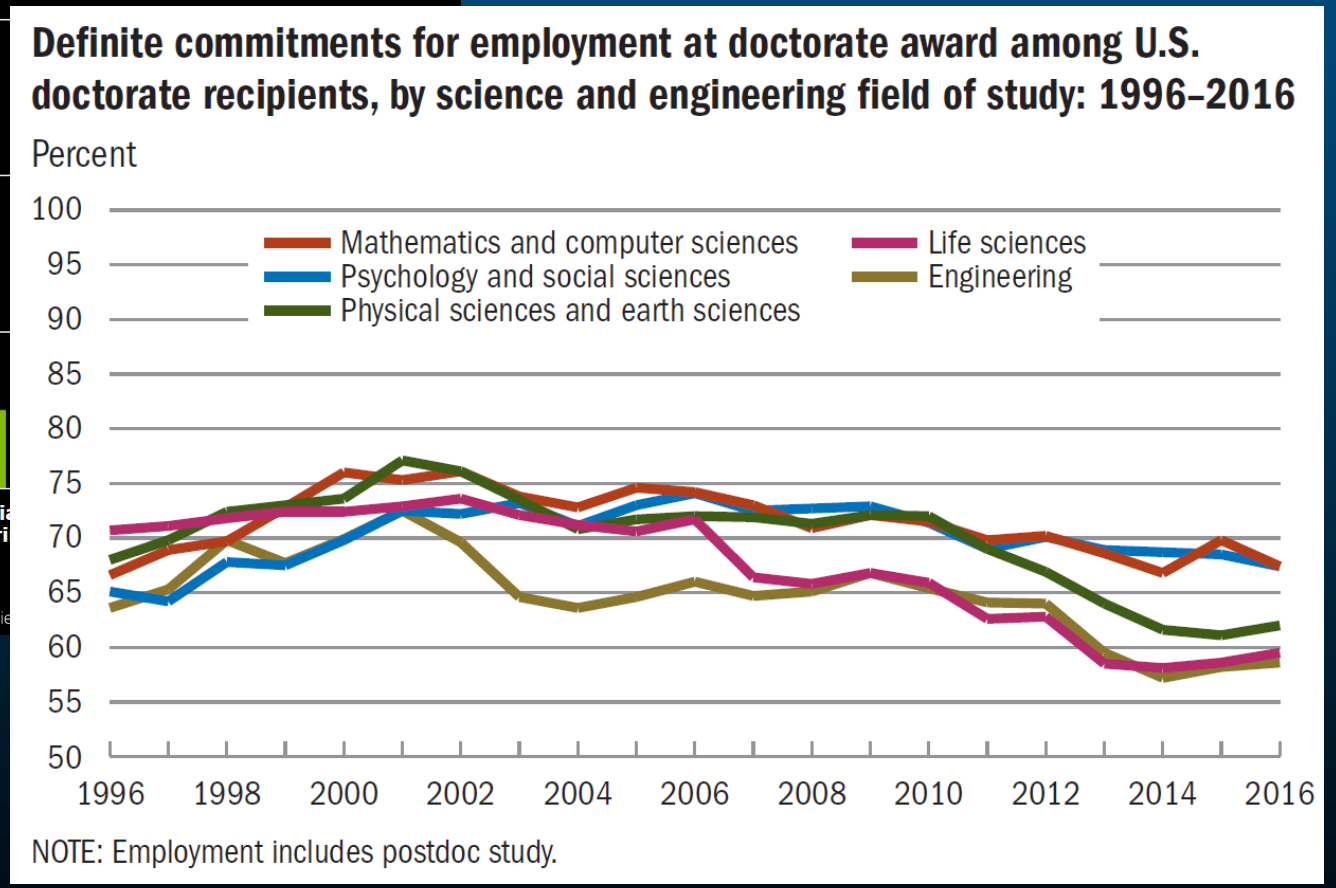
A mindset of agile learning on the part of both company leaders and workers will be needed, starting with an ability to re-imagine the routines and limits of today's jobs as part of a comprehensive workforce strategy for the Fourth Industrial Revolution.

-World Economic Forum Future of Jobs Survey, 2018

Skill Sets are Mismatched with Employer Needs

(SOURCE: DELOITTE, SEMI- ISS 2018 CONFERENCE; NSF STROBE, NSF 2018 SURVEY OF EARNED DOCTORATES)





Skills needed From Future Employees

Today, 2018	Trending, 2022	Declining, 2022
Analytical thinking and innovation	Analytical thinking and innovation	Manual dexterity, endurance and precision
Complex problem-solving	Active learning and learning strategies	Memory, verbal, auditory and spatial abilities
Critical thinking and analysis	Creativity, originality and initiative	Management of financial, material resources
Active learning and learning strategies	Technology design and programming	Technology installation and maintenance
Creativity, originality and initiative	Critical thinking and analysis	Reading, writing, math and active listening
Attention to detail, trustworthiness	Complex problem-solving	Management of personnel
Emotional intelligence	Leadership and social influence	Quality control and safety awareness
Reasoning, problem-solving and ideation	Emotional intelligence	Coordination and time management
Leadership and social influence	Reasoning, problem-solving and ideation	Visual, auditory and speech abilities
Coordination and time management	Systems analysis and evaluation	Technology use, monitoring and control

Source: Future of Jobs Survey 2018, World Economic Forum.

Employers are Expecting Multidisciplinary Capable Graduates

The Agile Learning Mindset- What Does This Mean?

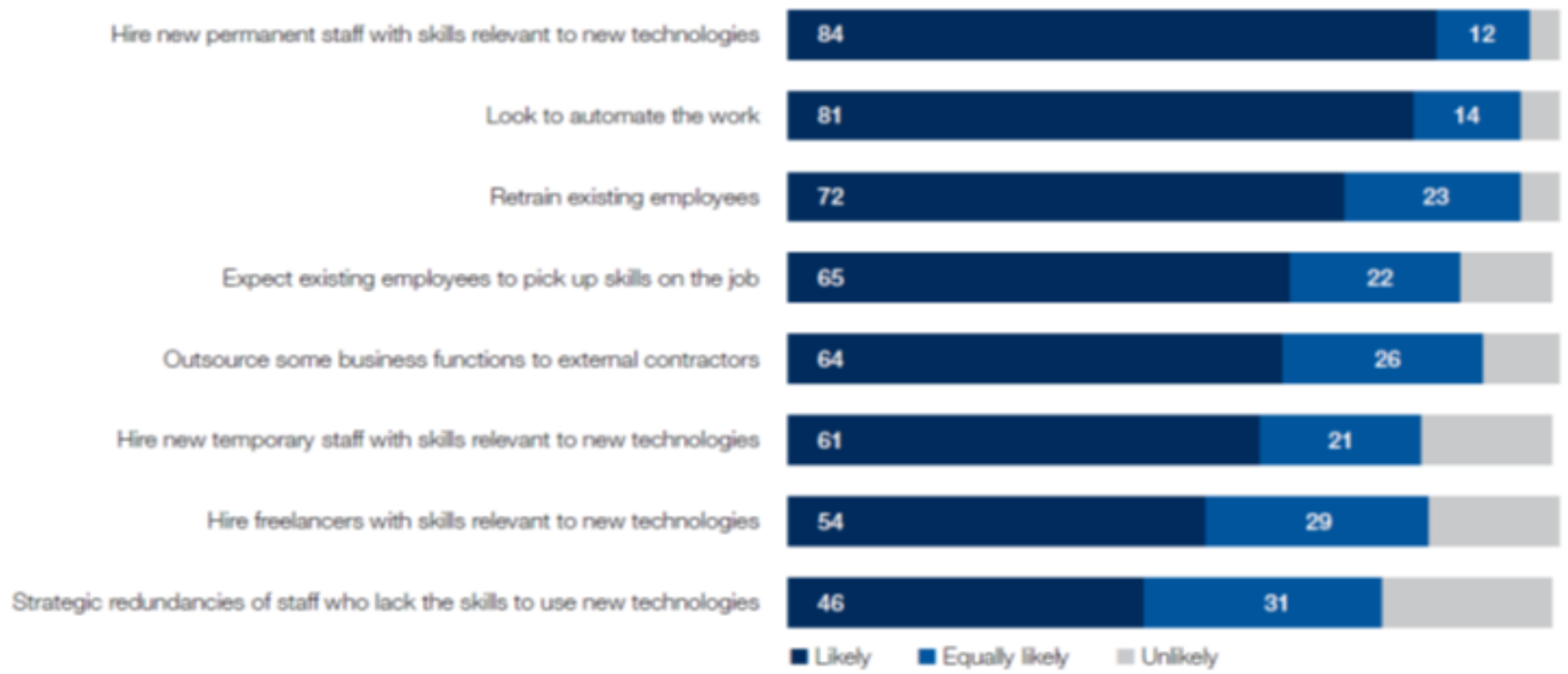
(Source: Strobe- 2018 NSF review; Institute for the Future, 2017; 2016 NSF Survey of Earned Doctorates)

- Life Long Learning
  - 85% of 2030 jobs that today's learners will be doing in 2030 have not yet been invented
  - Certificate programs, mini-degrees, apprenticeship programs needed to expeditiously learn new skills
- Meaningful research experiences/internships at both the grad and undergrad levels
- Partnerships in both directions of the education value chain
  - Much opportunity for University TAM Expansion with employer customized education (not training)
  - K-12 outreach to increase STEM pipeline
- Interdisciplinary approaches between university colleges and departments
  - Break down "Ivory Towers"
- Tenure requirements need to take into account performance to student outcomes
    - <15% of Engineering PhD's enter academia
    - Significant student debt on graduation

Academia has an Opportunity to take a Leading Role in Ensuring that the Fourth Industrial Revolution does not Accelerate Income Inequality

Employer Retraining Strategies

Figure 6: Projected (2022) strategies to address shifting skills needs, by proportion of companies (%)

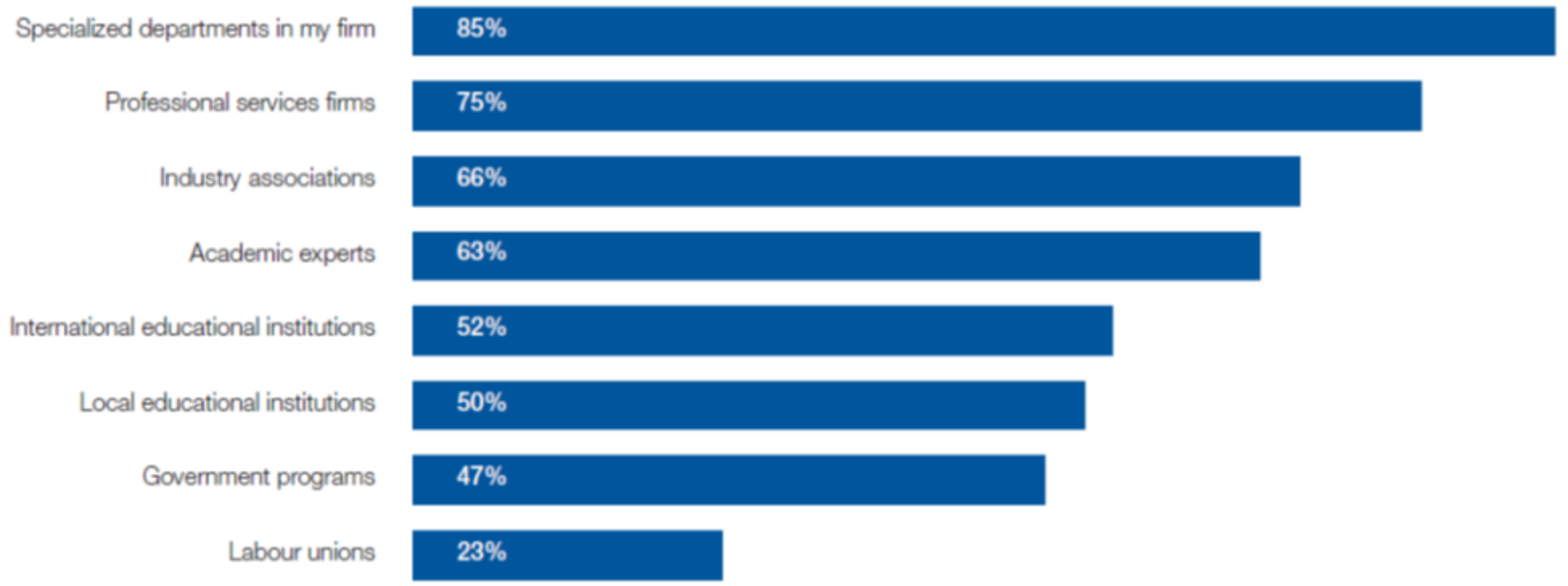


Source: Future of Jobs Survey 2018, World Economic Forum.

Note: The bars represent the proportion of responses by companies that stated that specific strategies were likely, equally likely or unlikely. Some companies abstained from answering the question. In such cases part of the bar remains blank (typically, 0–1% in the graph above).

Employers/Trade Organizations Want to Partner with Academia on Education Initiatives

Figure 8: Preferred partners in managing the integration of new technologies and workforce transition



Source: Future of Jobs Survey 2018, World Economic Forum.

Opportunities Exist for University TAM Expansion

Diversity: Call to Action

(Sources: STROBE, 2018; Herring, 2009; Kochan, 2003 and the Harvard Business Review)

- Innovation is enhanced by diversity
- BUT:
  - Discrimination takes the form of unconscious exclusion
    - Test your extent of bias at https://implicit.harvard.edu/implicit/selectatest.html
    - Harvard Business Review on promotable opportunities (https://hbr.org/2018/07/why-women-volunteer-for-tasks-that-dont-lead-to-promotions)
    - If you can't find anyone with the right qualifications, you haven't looked enough
  - Starts in middle school (at latest)
    - Outreach to K-12 is essential to improve pipeline of STEM students
  - Diverse students have already endured 5+ years of discrimination before getting to college

Reject Exclusion and Provide "Employable Opportunities" for ALL students

Summary

- Innovation Challenges are multidisciplinary and complex
- Education must adapt curricula and tenure requirements to prepare students
- Diversity drives improved outcomes

Acknowledgements

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Thank You!